Descriptions

The AP3216C is an integrated ALS & PS module that includes a digital ambient light sensor [ALS], a proximity sensor [PS], and an IR LED in a single package.

This device provides a multiple gain function with linear response over a dynamic range 365/1460/5840/23360 and is well suited to applications under clear glass or darkened glass.

The proximity function is targeted specifically towards near field application and detects external object with simple configurable zone controlled by registers. With multiple proximity gain control, multiple IR LED current control and 10-bit ADC output, this device is designed specially to fix low reflection objects, such as black hair.

The device supports an interrupt feature to improve system efficiency and several features that help to minimize the occurrence of false triggering. Through internal calibration and CMOS design, the AP3216C is designed to minimize device-to-device variations for ease of manufacturability.

Features

- I^2C interface (FS mode @ 400k Hz)
- Mode Select: ALS, PS+IR, ALS+PS+IR, PD, ALS once, SW Reset, PS+IR once and ALS+PS+IR once.
- Built-in temperature compensation circuit
- Wide operating temperature range (-30°C to +80°C)
- Ambient Light Photo Sensor
  - 16-bit effective linear output (0~65535)
  - 4 user selectable dynamic range
  - Anti-flicker rejection (reject 50/60Hz)
  - High sensitivity @ darkened glass
  - Window loss compensation
- Proximity Detector
  - 10 bit effective linear output (0~1023)
  - 4 programmable IR LED current output
  - High ambient light suppression
  - Cross talk compensation
- Form factor 4.1mm x 2.4 mm x 1.35 mm
- RoHS compliant

Applications

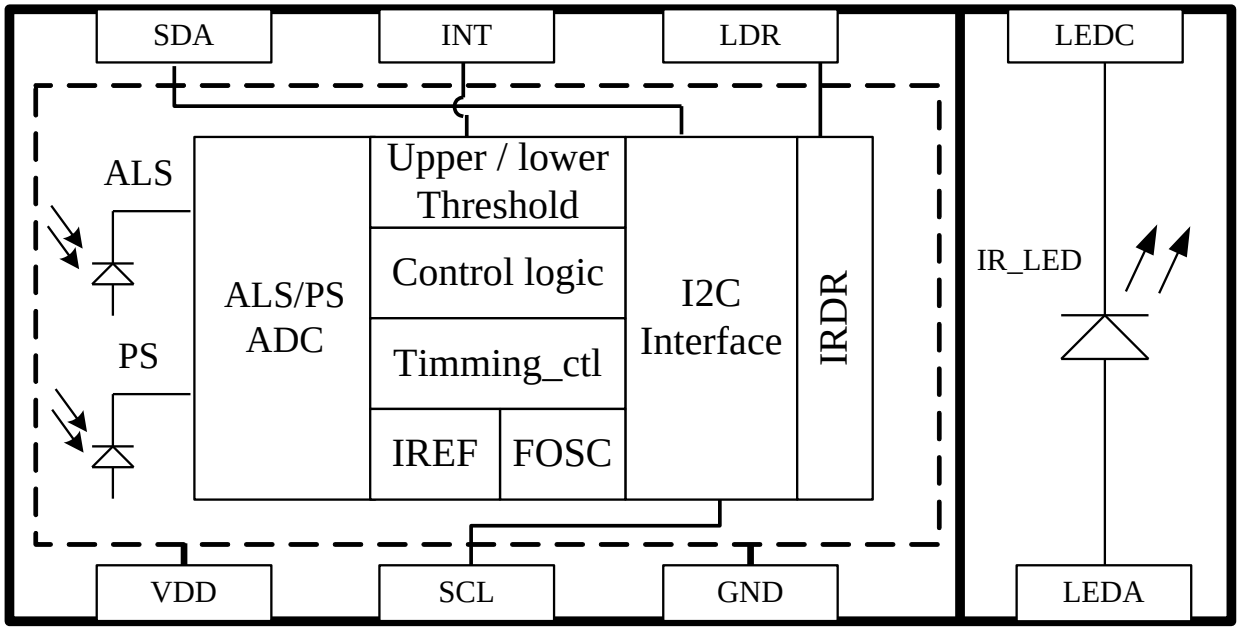
- Mobile phone, Pad
- Personal Navigation Device
- Notebook/Ultrabook
- LCD/PDP TV backlight systems
- Digital Photo Frame
- Applications with Capacitive Touch Panel

Ordering Information

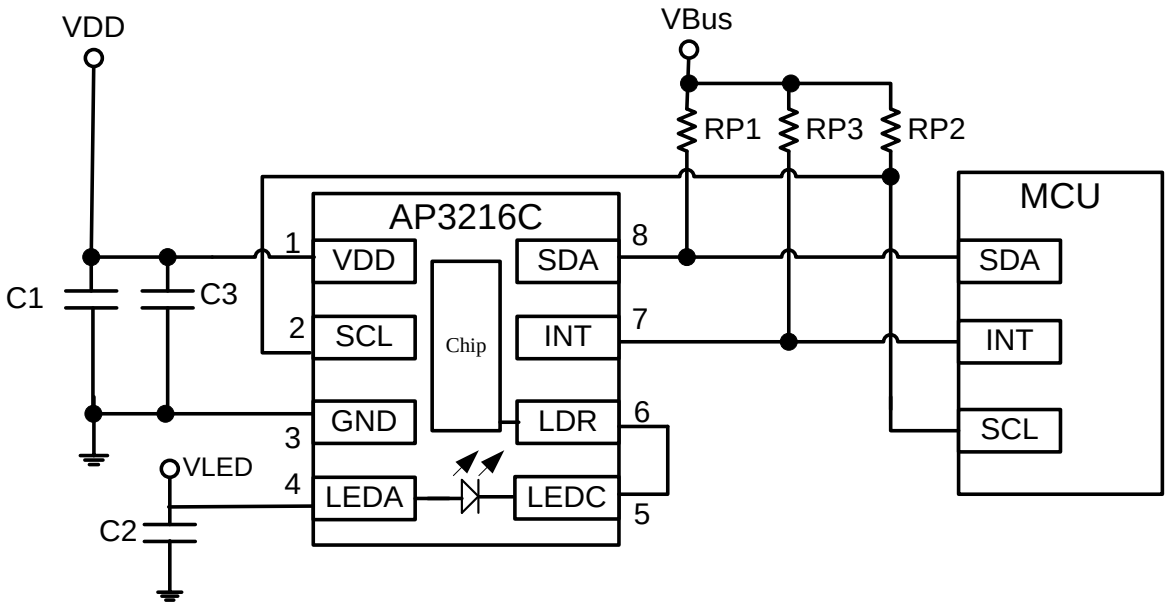
Part No.	Packing Type	Package	Quantity
AP3216C	Tape and Reel (MSL3)	8Ld Chipled 4.1 x 2.4 x 1.35mm	2,500

Please be aware that an **Important Notice** concerning availability, disclaimers, and use in critical applications of LSC products is at the end of this document.

Function Block Diagram



Typical Application Circuit



Recommended Application Circuit Components

Component	Recommended Value	Condition / Range
VLED	Depends on system design, connect to VDD or VBatt	
R_{p1}, R_{p2}	Depends on system design(*1)	
R_{p3}	Depends on system design	
C_1	1uF, ±20%	As close as possible to the sensor
C_2	2.2 uF, ±20%	As close as possible to the sensor
C_3(Optional)	0.1 uF, ±20%	As close as possible to the sensor

***Note 1: I^2C Pull up resistor for standard protocol format. For the complete description of maximum pull up resistor and minimum pull up resistor, please refer to: http://www.semiconductors.philips.com.**

Pin Descriptions

Pin Number	I/O Type	Pin Name	Description
1		VDD	Digital/Analog Power Supply
2	I	SCL	I^2C serial clock signal (open drain)
3		GND	Ground
4	I	LEDA	LED anode
5	O	LEDC	LED cathode
6	I	LDR	LED driver for proximity emitter
7	O	INT	Interrupt pin
8	I/O	SDA	I^2C serial data signal (open drain)

Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit
Supply Voltage 1	VDD	4.5	V
Supply Voltage 2	VLED	4.5	V
I^2C Bus Pin Voltage	SCL, SDA	-0.2 to 4.5	V
I^2C Bus Pin Current	SCL, SDA	10	mA
Operating Temperature	Tope	-40 to +85	℃
Storage Temperature	Tstg	-40 to +100	℃

***Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.**

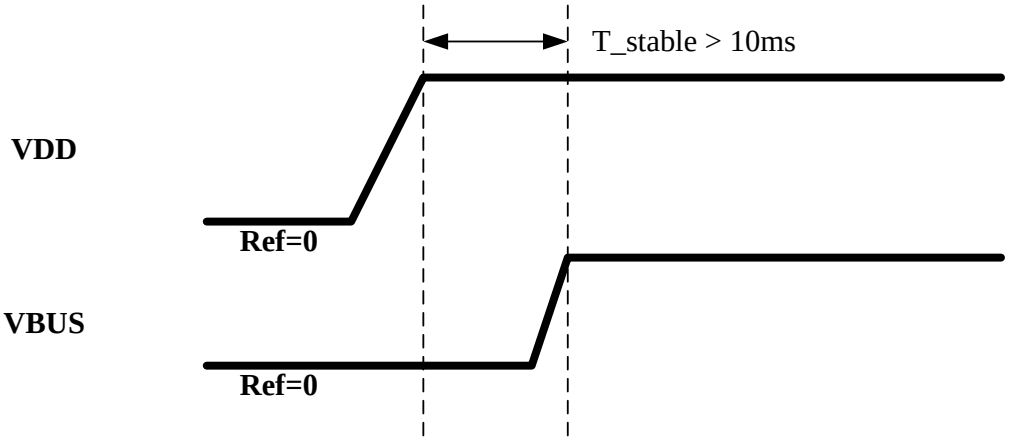
Recommended Operation Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage Note1	V_{DD}	2.4		3.6	V	
I^2C Bus Pin Voltage Note2	V_{Bus}	1.7		VDD	V	$V_{Bus} \leqq V_{DD}$
Operating Temperature	T_{ope}	-30		80	℃	
I^2C Bus Input High Voltage Note3	V_{IH_SCL}, V_{IH_SDA}	1.4			V	
I^2C Bus Input Low Voltage Note3	V_{IL_SCL}, V_{IL_SDA}			0.5	V	
SDA Output Low Voltage	V_{OL_SDA}	0		0.4	V	3mA sinking current
		0		0.6	V	6mA sinking current
INT Output Low Voltage	V_{OL_INT}	0		0.4	V	3mA sinking current

Notes:

1. Considering VDD rising time, please make sure a VDD slew rate at least 0.6V/ms. When the supply voltage drops out 10% of the recommended operation voltage range, please consider the low voltage detector that it is built-in IC internal to be brown out reset protection. When the VDD drops below 1.4V under room temp, the POR would be triggered and system will be reset. Then power of the chip will be recovered at the requirement slew rate, and write registers to the desired values.

2. If VDD and VBUS are supplied by different power source, please ensure the power sequence to avoid the reverse-voltage issue due to ESD protective diode.



3. The specs are defined under VDD=2.8V, T=25℃

Electrical & Optical Specifications

All specifications are at VDD=3.3V, T_{ope}=25℃, white light LED, unless otherwise noted.

Parameter		Symbol	MIN	TYP	MAX	Notes	UNIT
Active Supply Current Note1		Idd		170	250	Ev=0, excluding LED current	uA
Active Supply Current Note2		Idd		550	700	Ev=0, including LED current	uA
Shutdown Current		Ipd		2	5	Ev=0, I^2C inactive	uA
Ambient Light Sensor							
Dynamic Range	Range 1			23360		0.36 lux/count (Default)	lux
	Range 2			5840		0.089 lux/count	lux
	Range 3			1460		0.022 lux/count	lux
	Range 4			365		0.0056 lux/count	lux
ALS ADC Count	Range 1			360		Ev=128lux	count
	Range 2			1438		Ev=128lux	count
	Range 3			5750		Ev=128lux	count
	Range 4			23000		Ev=128lux	count
Dark Count					5	Ev=0, Range 4	count
Conversion Time				100		16bit ADC count	ms
Proximity Sensor							
LED Forward Voltage		V_F	1.3	1.45	1.6	I_F=20mA	V
LED Peak Wavelength		λp		850		I_F=20mA	nm
LED Spectral Bandwidth		Δλ		40		I_F=20mA	nm
PS Sensing Full Scale ADC Count (delta value)					1023		count
IR sensing Full Scale ADC Count (@ ambient light)					1023		count
Proximity ADC count value Note3				TBD			count
LED Driver Current 100% = 110mA @ Typ.				16.7			%
				33.3			%
				66.7			%
				100		Default	%

Notes:

1. The current consumption is tested under 0x00=0x03, 0x10=0x00, 0x20=0x59, 0x21=0x13, 0x23=0x00, 0x24=0x00 respectively, excluding LED current.

2. The current consumption is tested under 0x20=0x59, 0x21=0x13, 0x23=0x00, 0x24=0x07 respectively.

3. Test condition : 18% grey card, 43mm distance, register setting 0x20=0x79 & 0x21=0x13, open view(no glass) above the module.

Typical Performance Charts

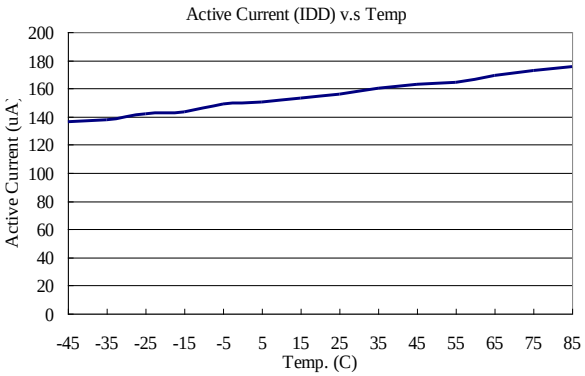


Fig.1 Active Current vs Temp

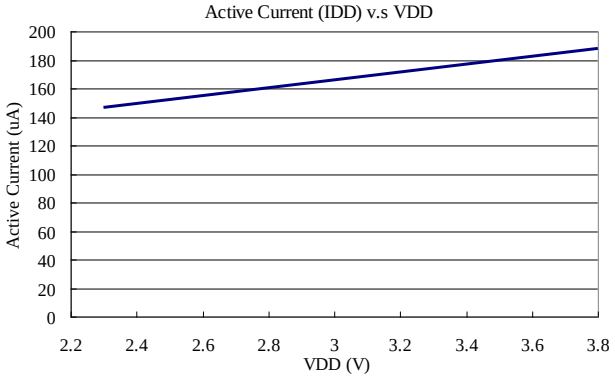


Fig.2 Active Current vs VDD

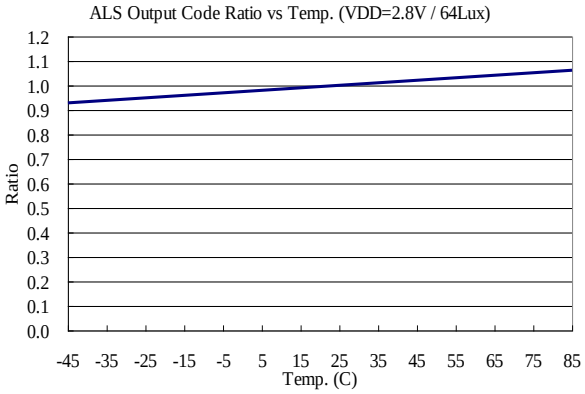


Fig.3 ALS Output Code Ratio vs Temp

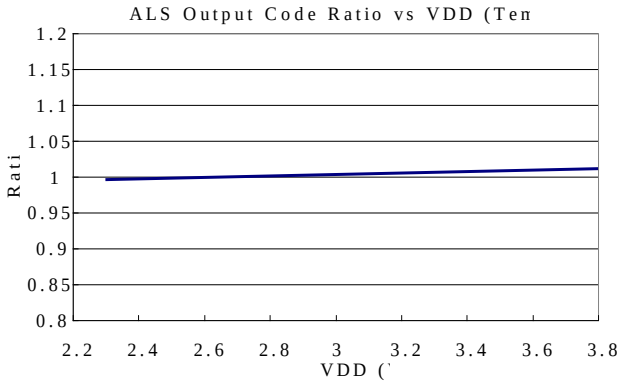


Fig.4 ALS Output Code Ratio vs VDD

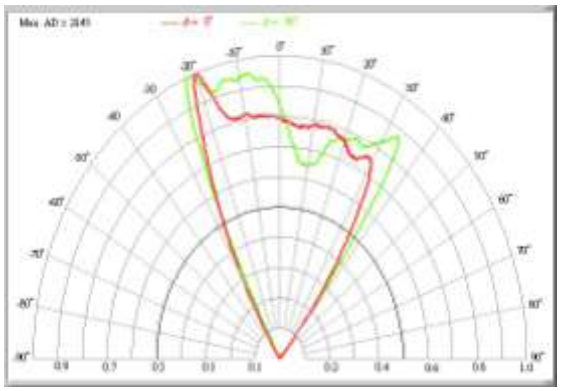


Fig.5 Angular Response of ALS

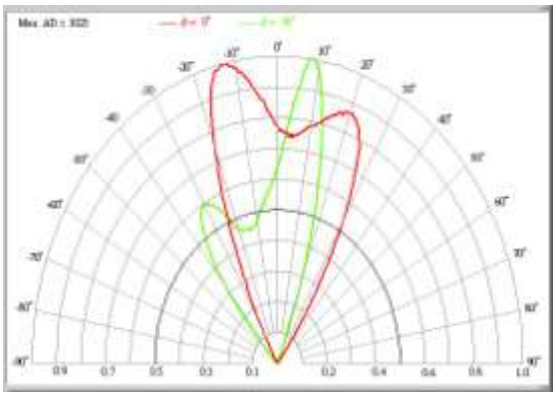


Fig.6 Angular Response of PS

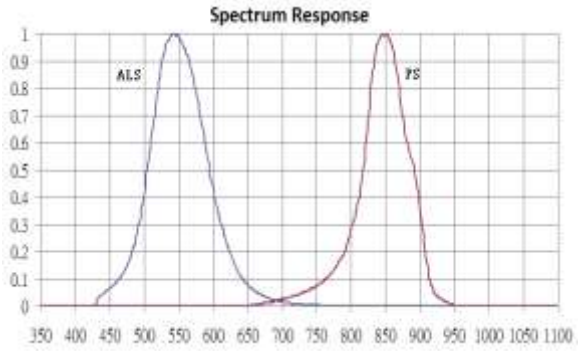


Fig.7 Spectrum Response

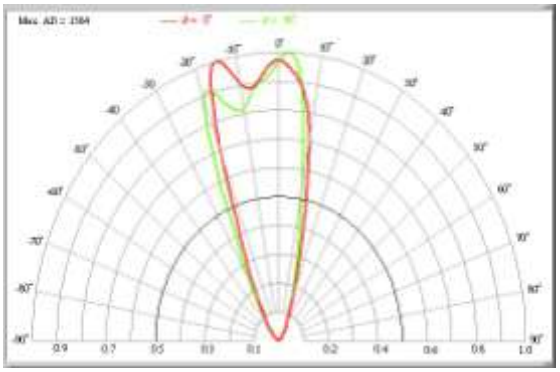
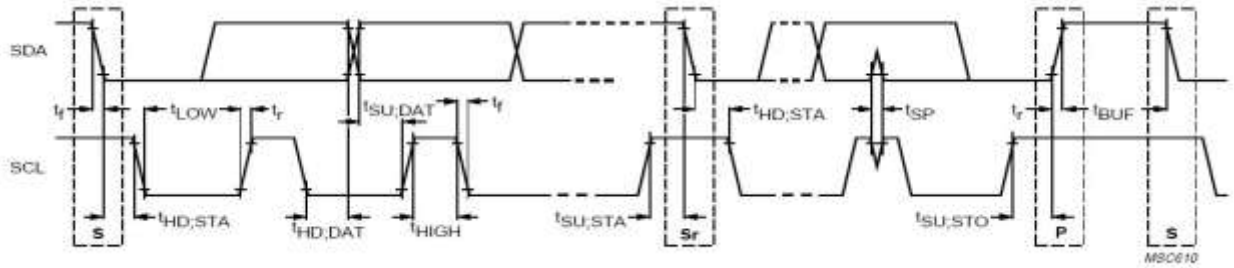


Fig.8 LED Emitting Angle

Definition of timing for I²C devices

This section will describe the main protocol of the I²C bus. For more details and timing diagrams, please refer to the I²C specification.



The device can operate at the standard mode I²C bus line or the fast mode I²C bus line. The characteristics of the I²C bus for difference modes are as bellow.

Characteristics of the SDA and SCL bus lines for I²C bus devices

Parameter (*)	Symbol	Fast mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	1	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3	--	us
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	--	us
LOW period of the SCL clock	t_{LOW}	1.3	--	us
HIGH period of the SCL clock	t_{HIGH}	0.6	--	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	--	us
Set-up time for STOP condition	$t_{SU;STO}$	0.6	--	us
Rise time of both SDA and SCL signals	t_r	$20 + 0.1C_b$ (note1)	300	ns
Fall time of both SDA and SCL signals	t_f	$20 + 0.1C_b$ (note1)	300	ns
Data hold time	$t_{HD;DAT}$	50	--	ns
Data setup time	$t_{SU;DAT}$	100	--	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns

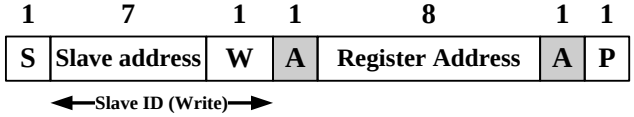
Note1: C_b (capacitance of one bus line) = 10~400(pF)

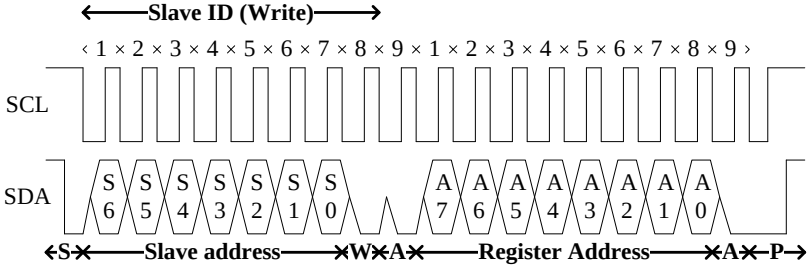
(*) Specified by design and characterization; not production tested.

(**) All specifications are at V_{Bus} = 3.3V, T_{ope}=25℃, unless otherwise noted.

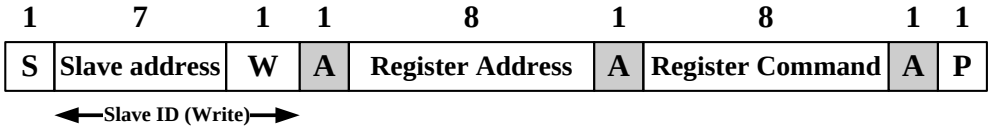
I²C Protocols

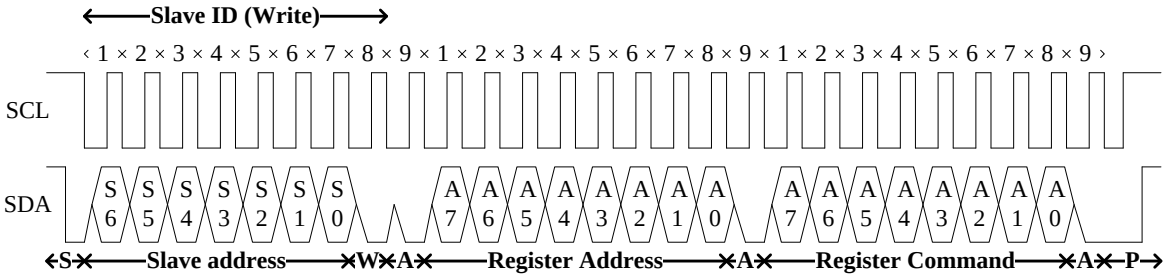
・I²C Write Protocol (type 1):



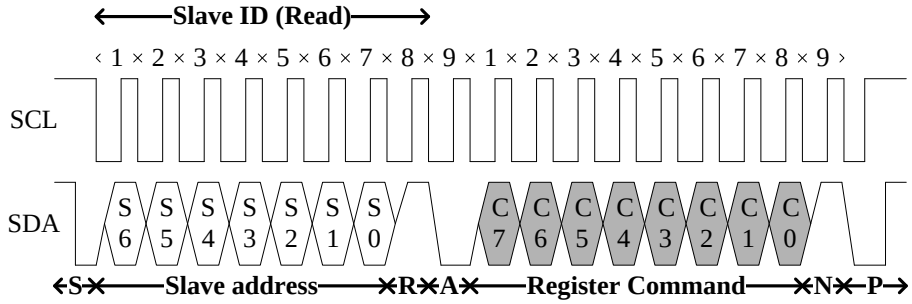


· I²C Write Protocol (type 2):

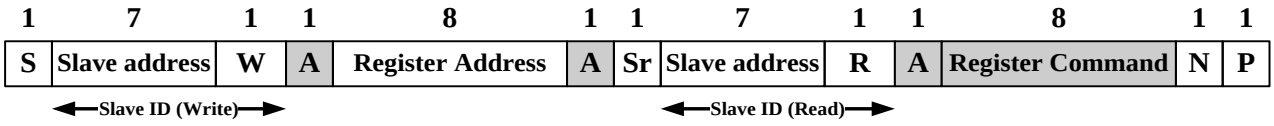


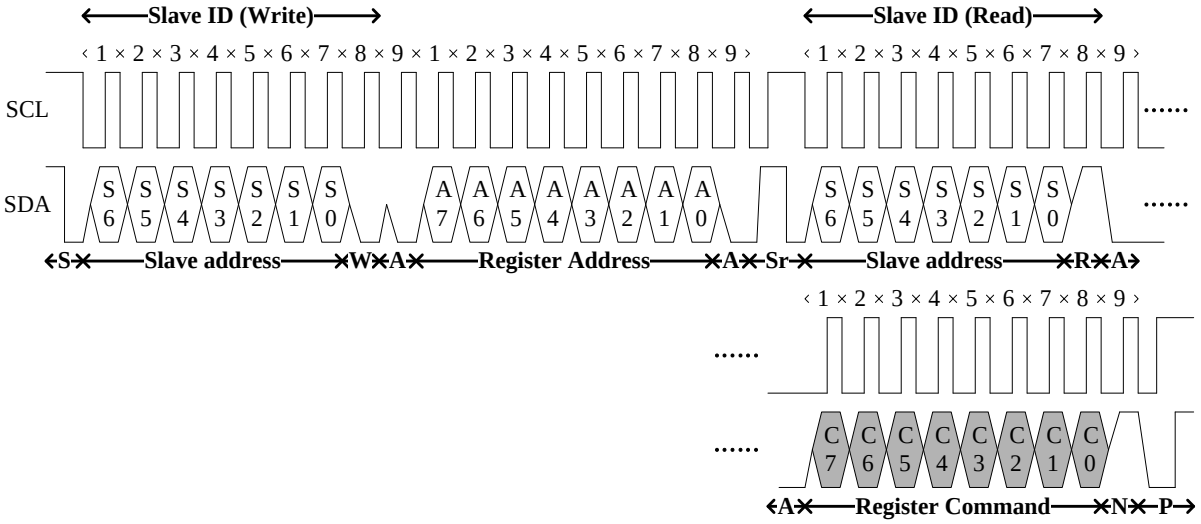


I²C Read Protocol:



· I²C Read (Combined format) Protocol:





A	Acknowledge (0 for an ACK)	**N**	Non-Acknowledge(1 for an NACK)
S	Start condition	**Sr**	Repeated Start condition
P	Stop condition		
W	Write (0 for writing)	**R**	Read (1 for read)
▒	Slave-to-master	□	Master-to-Slave

I²C Slave Address

The slave addresses have 7 bits. A read/write bit should be appended to the slave address by the master device to properly communicate with the device. The slave address of this device is 0x1E.

Register Table List

System Register Table

ADDR (HEX)	REGISTER NAME	DESCRIPTION
0x00	System Configuration	Control of basic functions
0x01	Interrupt Status	ALS and PS interrupt status output
0x02	INT Clear Manner	Auto/semi clear INT pin selector
0x0A	IR Data Low	Lower byte for IR ADC channel output
0x0B	IR Data High	Higher byte for IR ADC channel output
0x0C	ALS Data Low	Lower byte for ALS ADC channel output
0x0D	ALS Data High	Higher byte for ALS ADC channel output
0x0E	PS Data Low	Lower byte for PS ADC channel output
0x0F	PS Data High	Higher byte for PS ADC channel output

ALS Register Table

ADDR (HEX)	REGISTER NAME	DESCRIPTION
0x10	ALS Configuration	Control of gain, conversion time of persist for ALS
0x19	ALS Calibration	ALS window loss calibration
0x1A	ALS Low Threshold(7:0)	Lower byte of ALS low threshold
0x1B	ALS Low Threshold (15:8)	Higher byte of ALS low threshold
0x1C	ALS High Threshold (7:0)	Lower byte of ALS high threshold
0x1D	ALS High Threshold(15:8)	Higher byte of ALS high threshold

PS Register Table

ADDR (HEX)	REGISTER NAME	DESCRIPTION
0x20	PS Configuration	Control of gain, integrated time and persist for PS
0x21	PS LED Driver	Control of LED pulses number and driver current
0x22	PS INT Form	Interrupt algorithms style select of PS
0x23	PS Mean Time	PS average time selector
0x24	PS LED Waiting Time	Control PS LED waiting time
0x28	PS Calibration L	Offset value to eliminate cross talk
0x29	PS Calibration H	Offset value to eliminate cross talk
0x2A	PS Low Threshold (2:0)	Lower byte of PS low threshold
0x2B	PS Low Threshold (10:3)	Higher byte of PS low threshold
0x2C	PS High Threshold (2:0)	Lower byte of PS high threshold
0x2D	PS High Threshold (10:3)	Higher byte of PS high threshold

System Register Descriptions

ADDR (Hex)	REGISTER NAME	Bits	REGISTER COMMAND	FUNCTIONS/DESCRIPTION
0x00	System Configuration (Default : 0x00)	2:0	System Mode (Default : 000)	000: Power down (Default)
				001: ALS function active
				010: PS+IR function active
				011: ALS and PS+IR functions active
				100: SW reset
				101: ALS function once
				110: PS+IR function once
				111: ALS and PS+IR functions once
0x01	INT Status	1	PS Int (Read only) (Default : 0)	0: Interrupt is cleared or not triggered yet 1: Interrupt is triggered **Note1**
		0	ALS Int (Read only) (Default : 0)	0: Interrupt is cleared or not triggered yet 1: Interrupt is triggered **Note1**
0x02	INT Clear Manner	0	Clear Manner (Default : 0)	0: INT is automatically cleared by reading data registers 1: Software clear after writing 1 into address 0x01 each bit
0x0A	IR Data Low	7	IR overflow (Read only)	0: Valid IR and PS data 1: Invalid IR and PS data
		1:0	(Read only)	IR lower byte of ADC output
0x0B	IR Data High	7:0	(Read only)	IR higher byte of ADC output
0x0C	ALS Data Low	7:0	(Read only)	ALS lower byte of ADC output
0x0D	ALS Data High	7:0	(Read only)	ALS higher byte of ADC output
0x0E	PS Data Low	7	Object detect (Read only)	0: The object leaving 1: The object closed
		6	IR overflow (Read only)	0: Valid IR, PS data and object detected 1: Invalid IR, PS data and object detected
		3:0	(Read only)	PS lower byte of ADC output
0x0F	PS Data High	7	Object detect (Read only)	0: The object leaving 1: The object closed
		6	IR overflow (Read only)	0: Valid IR, PS data and object detected 1: Invalid IR, PS data and object detected
		5:0	(Read only)	PS higher byte of ADC output

Note1. The INT pin will be set low and set INT status bit when ALS or PS or (ALS+PS) interrupt event occurrence. User can clear INT bit and individual status bits when reading the register 0xD(ALS) , 0xF(PS) and 0xD+0xF(ALS+PS) respectively.

System Configuration Register

0x00	System Configuration (Default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*					*System Mode*		

The SYSTEM CONFIGURATION register is used to power up/down the device and to select the ALS and/or PS feature of the device.

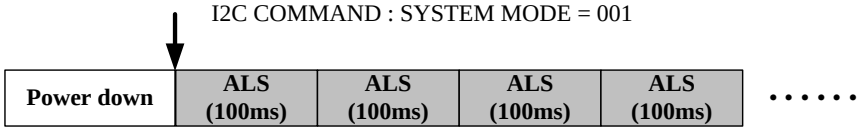
Field	BITS	Description
System mode	2:0	000: Power down (Default) 001: ALS function active 010: PS+IR function active 011: ALS and PS+IR functions active 100: SW reset 101: ALS function once 110: PS+IR function once 111: ALS and PS+IR functions once

For power down (000)

The device will stop operation. The register will keep previous settings although the device sleeps. The ALS, PS and IR will be cleared.

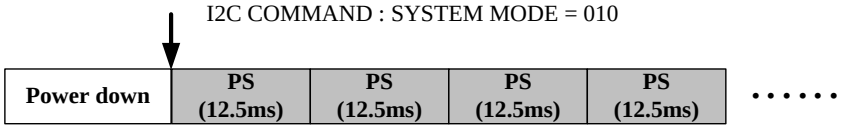
For ALS function active (001)

The device will operate only for ALS function. The typical conversion time of ALS is 100ms. The PS data will not work at this mode. The operation time is showed as below :



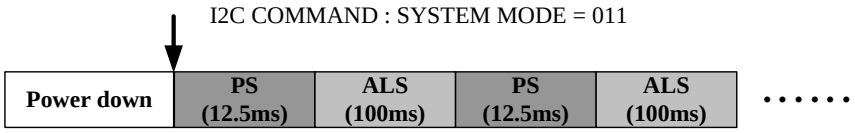
For PS+IR function active (010)

The device will operate only for PS+IR function. The typical conversion time of IR is 12.5ms, and the PS is decided by the PS waiting time. The ALS data will not work at this mode. The operation time is showed as below (PS waiting time = 0):



For ALS and PS+IR functions active (011)

The device will operate the ALS and PS+IR function alternately. The conversion time will be double at this mode. The operation time is showed as below (PS waiting time = 0) :

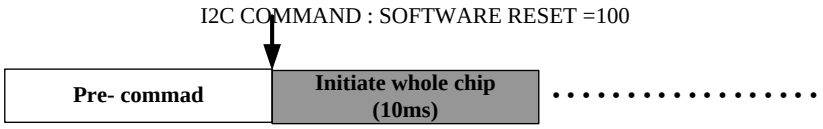


The conversion time of difference modes are listed as below.

System Mode	Conversion Time (Typical Value)		
	ALS	PS	IR
ALS	100ms	~	~
PS+IR	~	(PS wait time + 1) * 12.5ms	12.5ms
ALS+PS+IR	112.5ms	(PS wait time + 1) * 112.5ms	112.5ms

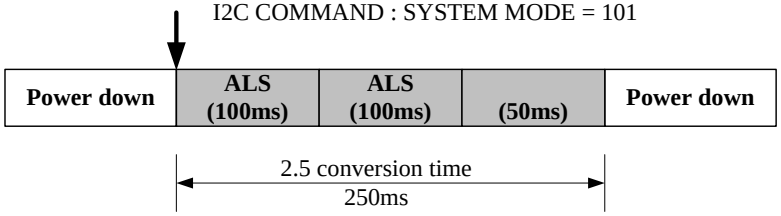
For SW reset (100)

When the host writes this setting, the all registers of device will become the default value after 10ms. Please don't force command during these period of 10ms to avoid abnormal operation



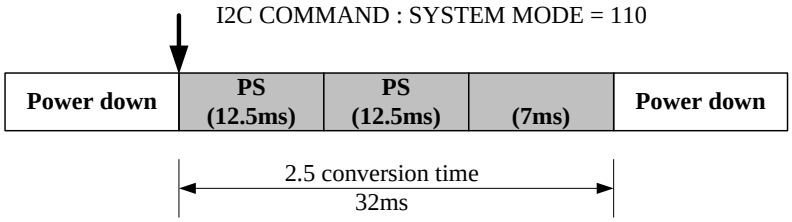
For ALS function once (101)

When the host writes this setting, the device will work at ALS mode in a short time. Then the device will become power down automatically after the device gets the ALS data. This time is typically 2.5 conversion time. If the device is slept by the ALS once command, the ALS data will be kept and not cleared.



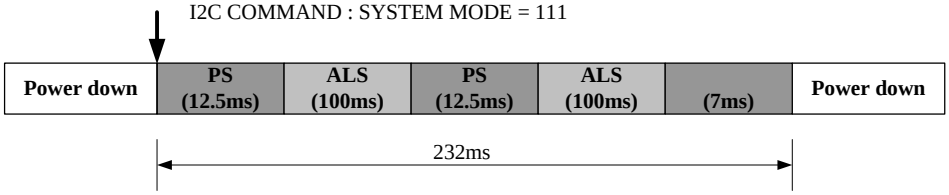
For PS+IR function once (110)

When the host writes this setting, the device will work at PS mode in a short time. Then the device will become power down automatically after the device gets the PS and IR data. This time is typically 2.5 conversion time and is not affected by the PS waiting. If the device is slept by the PS once command, the PS and IR data will be kept and not cleared.



For ALS and PS + IR function once (111)

When the host writes this setting, the device will operate the ALS and PS+IR function alternately in a short time. Then the device will become power down automatically after the device gets the ALS, PS and IR data. This time is typically 232ms and is not affected by the PS waiting. If the device is slept by this once command, the ALS, PS and IR data will be kept and not cleared.



INT Status Register

0x01	ALS and PS Interrupt Status Register (Default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
W/R	*Reserved*						*PS INT*	*ALS INT*

The ALS INT bit register is used to indicate the ALS interrupt be triggered (set to 1) or not (set to 0). It will be cleared after 0x0D register be read or write 0x01 to clear (depend on INT Clear Manner flag).

The PS INT bit register is used to indicate the PS interrupt be triggered (set to 1) or not (set to 0). It will be cleared after 0x0F register be read or write 0x02 to clear (depend on INT Clear Manner flag).

INT Clear Manner Register

0x02	INT Clear Manner Register (Default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
W/R	*Reserved*							*CLR_MNR*

In order to provide the multiple control flow with interrupt flag handling, The CLR_MNR bit used to assign two manners of interrupt status flag de-asserted. It is set to 0, the interrupt flag be automatic cleared by reading data registers (0x0C, 0x0D, 0x0E, 0x0F). On the other hand, the interrupt flag is cleared by write 1. For example, if PS_INT asserted, it can be cleared after I^2C write address 0x01 with 0x02.

IR Data Register

0x0A	IR Data Low							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
W/R	*IR_OF*	*Reserved*					*IR Data Low*	

0x0B	IR Data High							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*IR Data High*							

The ADC channel data for IR is expressed as 10-bit data spreading across two registers, IR Data Low and ID Data High. These two will provide the lower and higher bytes of the ADC value respectively. The IR DATA can show the intensity of environment IR. All channel data registers are read-only.

If the IR is high intensity, it will affect the PS data and cause the PS data invalid. There is an overflow flag (IR_OF) to indicate the PS data to see if it is valid or not in high IR light. If the IR_OF is set to 1, the device will force the PS object status as away state..

The higher byte registers can be read after reading the lower byte register. When the lower byte register is read, the higher byte is stored in a temporary register, which is read by a subsequent read to the higher byte. The higher byte register will read the correct value even if additional integration cycles end between the reading of the lower and higher byte data registers.

ALS Data Register

0x0C	ALS Data Low							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*ALS Data Low*							

0x0D	ALS Data High							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*ALS Data High*							

The ADC channel data for ALS is expressed as 16-bit data spread across two registers, ALS Data Low and ALS Data High. These two will provide the lower and higher bytes of the ADC value respectively. All channel data registers are read-only.

The higher byte registers can be read after reading the lower byte register. When the lower byte register is read, the higher byte is stored in a temporary register, which is read by a subsequent read to the higher byte. The higher byte register will read the correct value even if additional integration cycles end between the reading of the lower and higher

byte data registers.

PS Data Register

0x0E	PS Data Low							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*OBJ*	*IR_OF*	*Reserved*	*Reserved*	*PS Data Low*			

0x0F	PS Data High							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
RO	*OBJ*	*IR_OF*	*PS Data High*					

The ADC channel data for PS is expressed as 10-bit data spread across two registers, PS Data Low and PS Data High. These two will provide the lower and higher bytes of the ADC value respectively.

The PS object status (OBJ) bit shows the position of object. When object is away from sensor and the count of PS across the threshold of PS, the OBJ bit will be reset to 0. On other way, the object is near the sensor and OBJ bit set to 1 to indicate object closed.

The IR overflow flag (IR_OF) indicates the PS data valid or not. If this bit is set to 1, it indicates that the data of PS is invalid in high intensive IR light. Please refer to description of IR data register.

The higher byte registers can be read after reading the corresponding lower byte register. When the lower byte register is read, the higher byte is stored in a temporary register, which is read by a subsequent read to the higher byte. The higher byte register will read the correct value even if additional integration cycles end between the reading of the lower and higher byte data registers. All channel data registers are read-only.

ALS Register Descriptions

ADDR (Hex)	REGISTER NAME	Bit	REGISTER COMMAND	FUNCTIONS/DESCRIPTION
0x10	ALS Configuration (Default : 0x00)	5:4	ALS dynamic range (Default : 00)	00: 20661 lux (Default) 01: 5162 lux 10: 1291 lux 11: 323 lux
		3:0	ALS persist (Interrupt filter) (Default : 0000)	ALS interrupt is triggered after N conversion time 0000: 1 conversion time (Default) 0001: 4 conversion time 0010: 8 conversion time 0011: 12 conversion time 0100: 16 conversion time …… 1111: 60 conversion time
0x19	ALS Calibration (Default : 0x40)	7:0	ALS window loss calibration (Default : 0x40)	0x00: calibration factor = 0/64 …… 0x40: calibration factor = 64/64 …… 0xFF: calibration factor = 255/64
0x1A	ALS Low Threshold L (Default : 0x00)	7:0		Lower byte of low interrupt threshold for ALS
0x1B	ALS Low Threshold H (Default : 0x00)	7:0		Higher byte of low interrupt threshold for ALS
0x1C	ALS High Threshold L (Default : 0xFF)	7:0		Lower byte of high interrupt threshold for ALS
0x1D	ALS High Threshold H (Default : 0xFF)	7:0		Higher byte of high interrupt threshold for ALS

ALS Configuration Register

0x10	**ALS Configuration (Default = 0x00)**							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*		*ALS Gain*		*ALS Interrupt Filter*			

The ALS Configuration register is used to set ALS gain and ALS interrupt filter (persist).

1. ALS Gain (Ambient light detectable range). There are 4 ranges below for AP3216C.
   A. Range 1 (B5B4=’00’): 0 ~ 20661 Lux. Resolution = 0.35 lux/count.
   B. Range 2 (B5B4=’01’): 0 ~ 5162 Lux. Resolution = 0.0788 lux/count.
   C. Range 3 (B5B4=’10’): 0 ~ 1291 Lux. Resolution = 0.0197 lux/count.
   D. Range 4 (B5B4=’11’): 0 ~ 323 Lux. Resolution = 0.0049 lux/count

   ALS ADC data to Lux conversion formula as below

   Ambient Light (lux) = 16 bit ALS ADC data * Resolution
2. ALS Interrupt Filter: Configurable interrupt filtering is to provide hardware interrupt to be generated after interrupts trigger for N consecutive numbers of conversion time. The ALS interrupt filter bits determine N.

There are 4 bits settings could be selected, for example :

1. B3B2B1B0=’0000’, N = 1
2. B3B2B1B0=’0001’, N = 4
3. B3B2B1B0=’0010’, N = 8
4. B3B2B1B0=’0011’, N = 12
5. B3B2B1B0=’0100’, N = 16
6. B3B2B1B0=’1111’, N = 60

ALS Calibration Register

0x19	**ALS Calibration (Default = 0x40)**							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS Calibration*							

To compensate ALS window loss induced from assembly, the device provide a parameter port to setup a value to eliminate the difference between each component. It is a floating point number with effective range from 0 ~3.98. The 8bits register presents 00.000000(0.00) ~11.111111 (3.98) and it’s resolution is 1/64. If it is wrote by 0x50 then it is equivalent to 1.25 (80* 1/64).

For example :

1. Original ALS data (component level) = 1000 counts
2. After assembly ALS data = 800 counts
3. Window loss should be compensated = 1000/800=1.25
4. The register should be set to 0x50 (80*1/64=1.25)

ALS ADC Low Threshold Register (Read/Write)

0x1A	**ALS Low Threshold Lower Byte (Default = 0x00)**							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS Low Threshold Lower byte*							

0x1B	**ALS Low Threshold Higher Byte (Default = 0x00)**							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS Low Threshold Higher byte*							

The ALS Low Threshold registers store the values of the low threshold data. An interrupt is triggered when ALS ADC (Registers 0CH & 0DH) < ALS ADC Low Threshold.

ALS ADC High Threshold Register (Read/Write)

0x1C	ALS High Threshold Lower Byte (Default = 0xFF)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS High Threshold Lower byte*							

0x1D	ALS High Threshold Higher Byte (Default = 0xFF)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*ALS High Threshold Higher byte*							

The ALS High Threshold registers store the values of the high threshold data. An interrupt is triggered when ALS ADC (Registers 0CH and 0DH) > ALS ADC High Threshold.

PS Register Descriptions

ADDR (Hex)	REGISTER NAME	Bit	REGISTER COMMAND	FUNCTIONS/DESCRIPTION
0x20	PS Configuration (Default : 0x05)	7:4	PS / IR Integrated time select (Default : 0000)	0000: 1T (Default) 0001: 2T …… 1111: 16T
		3:2	PS gain (Default : 01)	00: 1 01: 2 (Default) 10: 4 11: 8
		1:0	PS persist (Interrupt filter) (Default : 01)	PS interrupt is triggered after N conversion time 00: 1 conversion time 01: 2 conversion time (Default) 10: 4 conversion time 11: 8 conversion time
0x21	PS LED Control (Default : 0x13)	5:4	LED pulse (Default : 01)	00: 0 pulse 01: 1 pulse (Default) 10: 2 pulses 11: 3 pulses
		1:0	LED driver ratio Typ. 100% = 110mA (Default : 11)	00: 16.7% 01: 33.3% 10: 66.7% 11: 100% (Default)
0x22	PS INT Mode (Default : 0x01)	0	PS_Algo (Default : 1)	0: PS INT Mode 1 (Zone type) 1: PS INT Mode 2 (Hysteresis type, default)
0x23	PS mean time (Default : 0x00)	1:0	Edit PS mean time (Default : 00)	00 : mean time=12.5ms (Default) 01 : mean time=25ms 10 : mean time=37.5ms 11 : mean time=50ms
0x24	PS LED Waiting (Default : 0x00)	5:0	PS LED waiting (Default : 0x00)	0x0 : 0, no waiting (Default) 0x1 : 1 mean time 0x2 : 2 mean times

				…… 0x3F : 63 mean times
0x28	PS Calibration L (Default : 0x00)	0	PS calibration	Lower byte of PS calibration
0x29	PS Calibration H (Default : 0x00)	7:0	PS calibration	Higher byte of PS calibration
0x2A	PS Low Threshold L (Default :0x00)	1:0		Lower byte of low interrupt threshold for PS
0x2B	PS Low Threshold H (Default :0x80)	7:0		Higher byte of low interrupt threshold for PS
0x2C	PS High Threshold L (Default :0x00)	1:0		Lower byte of high interrupt threshold for PS
0x2D	PS High Threshold H (Default :0x80)	7:0		Higher byte of high interrupt threshold for PS

PS Configuration Register

0x20	**PS Configuration (Default = 0x05)**							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*PS/IR Integration time*				*PS Gain*		*PS Interrupt Filter*	

The PS Configuration register is used to set PS integration time, PS gain, LED waiting time and PS interrupt filter. The PS integration time sets ADC's sample/conversion time and it will affect both resolution and sensitivity. Longer integration time increases IR ADC&PS ADC resolution and sensitivity.

PS integration time (bits 7:4)	PS ADC and IR ADC resolution
0000 (1T) (Default)	X1
0001 (2T)	X2
1110 (15T)	X15
1111 (16T)	X16

The PS gain setting can be used to increase/decrease the OBJ's detection distance. Higher gain can increase detection distance but also increase noise or cross talk signal. The IR ADC will not be affected.

PS gain (bits 3:2)	PS resolution
00	X1
01 (Default)	X2
10	X4
11	X8

The PS interrupt filter prevents the interrupt triggered by noises. The interrupt is triggered when the PS object status has changed and keeps the change for M consecutive number of conversion time. The PS interrupt filter bits determine the M.

PS interrupt filter (bits 1:0)	Number of "M" conversion time
00	1
01 (Default)	2
10	4
11	8

PS LED Control Register

0x21	**PS LED Control (Default = 0x13)**							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*		*LED pulse*		*Reserved*		*Max LED driver ratio*	

The PS LED Control register is used to control IR LED.

The LED pulse bits set the number of PS pulses that will be transmitted in one PS conversion time. More pulses increase LED current consumption but also increase the PS detection distance.

LED pulse selection (bits 5:4)	Number of pulse(s)
00	0
01 (Default)	1
10	2
11	3

The LED driver ratio sets the max current on the LED driver. Higher ratio increases LED current consumption but also increase the PS detection distance.

Max LED driver ratio (bits 1:0)	Percentage of max LED current
00	16.7%
01	33.3%
10	66.7%
11 (Default)	100%

PS Interrupt Mode Register

0x22	PS Interrupt Mode (Default = 0x01)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	Reserved							PS_Algo

The PS_Algo bit is used to set PS interrupt mode. There are two behavior algorithms can be selected.

B0	PS Interrupt mode
0	PS INT Mode 1 (Zone type)
1 (Default)	PS INT Mode 2 (Hysteresis type)

Mode 1 interrupt behavior is shown as Fig1. High/low absolute threshold are set at beginning. If PS DATA is increased/decreased cross the high/low threshold and kept over N(1~8) persist times, an interrupt will be triggered. When each interrupt is asserted, the host can de-assert INT pin by read E/F register and then host shall set another new high/low absolute threshold specified for next time interrupts. The PS threshold is set by the register 0x2A / 0x2B / 0x2C / 0x2D.

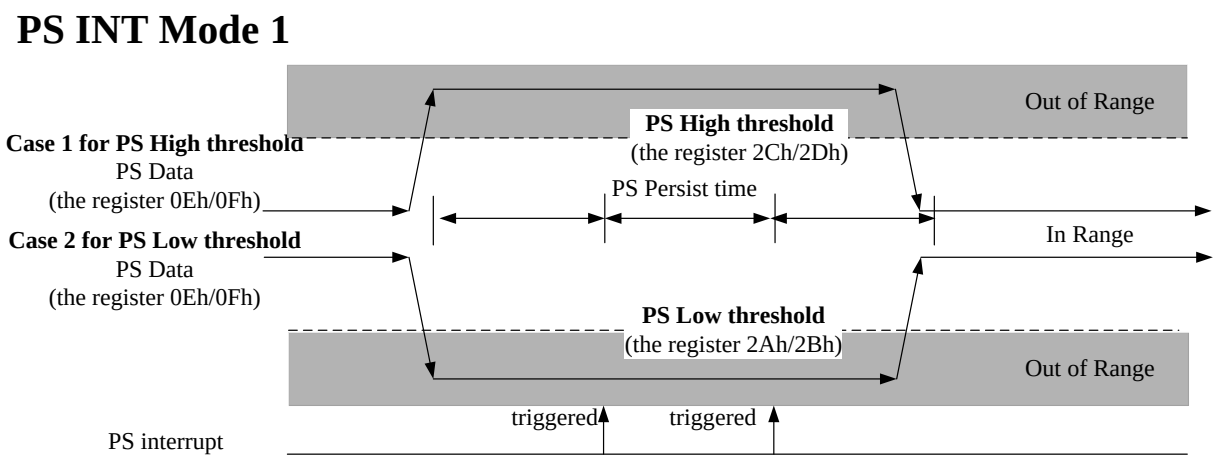
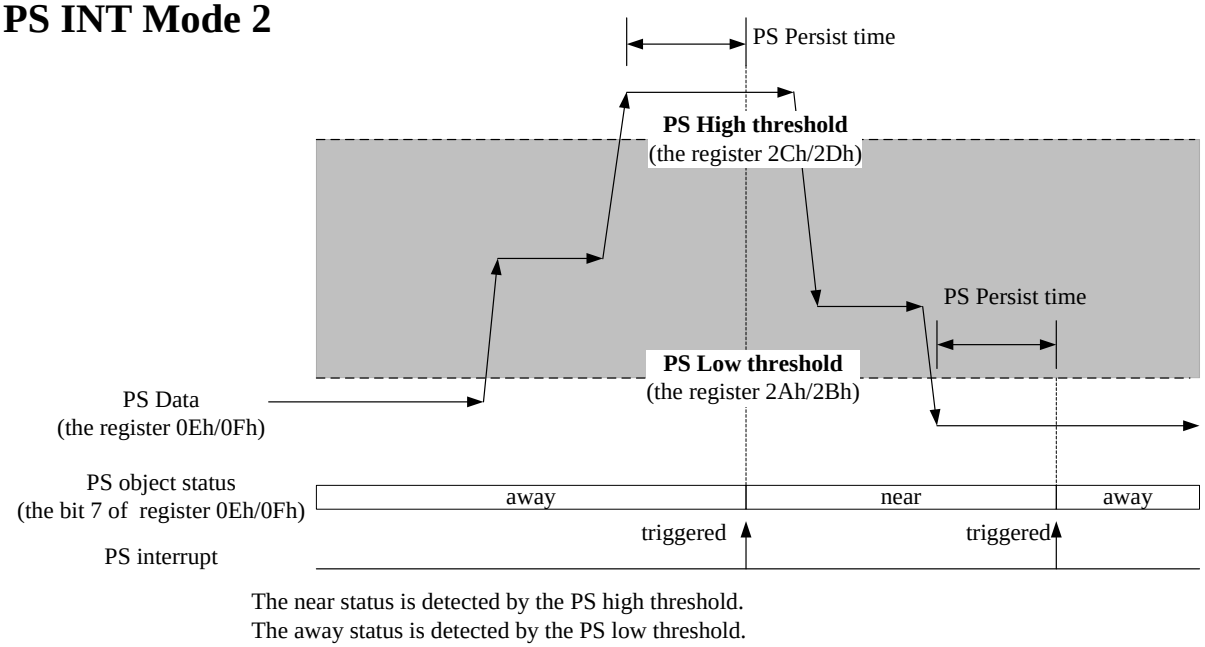


Fig1. The behavior of PS INT mode 1 with control flow diagram.

Mode 2 performs a hysteresis behavior. Assume the PS object status is “near”, PS interrupt will be triggered only if the PS data is cross below the PS low threshold (The interrupt is triggered when PS object status changed). On the other hand, assume the PS object status is “away”, PS interrupt will be triggered only if the PS data is cross above the PS high threshold. The PS threshold can be set by the register 0x2A / 0x2B / 0x2C / 0x2D.

PS INT Mode 2



The near status is detected by the PS high threshold.
The away status is detected by the PS low threshold.

Fig2. The behavior of PS INT mode 2 with control flow diagram.

PS Mean Time Register

0x23	PS Mean Time (Default=0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*						*Mean_time*	

This control bits are used to setup the PS integrated time.

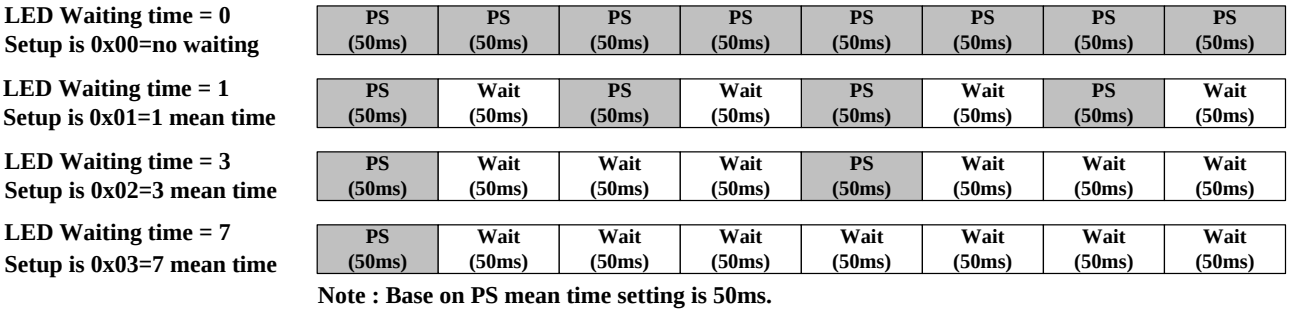
1. B1B0=’00’, 1 time (mean time =12.5ms) (Default)
2. B1B0=’01’, 2 time (mean time =25ms)
3. B1B0=’10’, 3 time (mean time =37.5ms)
4. B1B0=’11’, 4 time (mean time =50ms)

PS LED Waiting Time Register

0x24	PS LED Waiting Time (Default=0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*			*PS LED Waiting*				

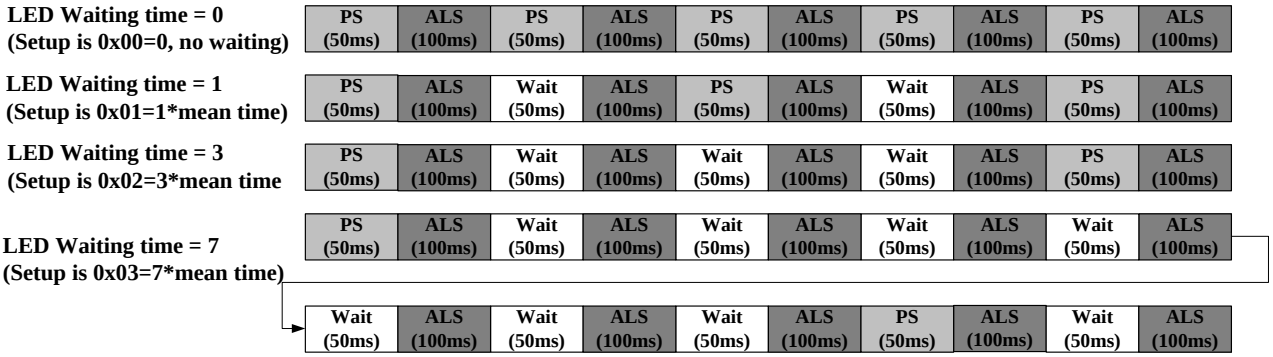
The PS waiting time sets LED’s ON/OFF time and it also affects proximity sensor’s response time. It can save system’s power consumption by setting longer waiting time but it increases response time to the system as well. The timing chart of PS waiting time is showed as below.

PS waiting time for PS mode



Note : Base on PS mean time setting is 50ms.

PS waiting time for ALS + PS mode



Note : Base on PS mean time setting is 50ms.

Longer PS waiting time increases the PS conversion time as well. Table for PS waiting time vs conversion time is showed as below. The PS conversion time will be set by the PS waiting time (base on PS mean time setting=50ms).

PS waiting time (bits 4:0)	Conversion time for PS	Conversion time for ALS + PS
0 (Default, no waiting)	50ms	150ms
1 (1 PS mean time)	100ms	300ms
2 (2 PS mean time)	150ms	450ms
…	…	…
63 (63 PS mean time)	3200ms	9600ms

PS Calibration Register

0x28	PS Calibration Lower Byte (Default=0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*							*PS_Cal[0]*

0x29	PS Calibration Higher Byte (Default=0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*PS_Cal[8:1]*							

Similar to ALS calibration for window loss compensation, the device also has PS calibration which could be used to eliminate the differences of cross talk which is induced from top cover/glass after assembly. Total 9bits dynamic range is available for resetting the cross talk to let the PS count indicates the distance directly. It is convenient for users to set the same PS high/low threshold regardless individual difference between each device.

PS Low Threshold Register

0x2A	PS Low Threshold Lower Byte (Default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*						*PS Low Threshold Lower Byte*	

0x2B	PS Low Threshold Higher Byte (Default = 0x80)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*PS Low Threshold Higher Byte*							

PS High Threshold Register

0x2C	PS High Threshold Lower Byte (Default = 0x00)							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*Reserved*						*PS High Threshold Lower Byte*	

0x2D	PS High Threshold Higher Byte (Default = 0x80)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
R/W	*PS High Threshold Higher Byte*							

The PS Threshold registers store the values of the high and low trigger points for comparison against PS DATA (Registers 0x0E and 0x0F). The host can decide what kind of the PS interrupt behavior by setting the PS INT FORM (Register 0x22) and the PS High/Low Threshold (Register 0x2A / 0x2B / 0x2C / 0x2D).

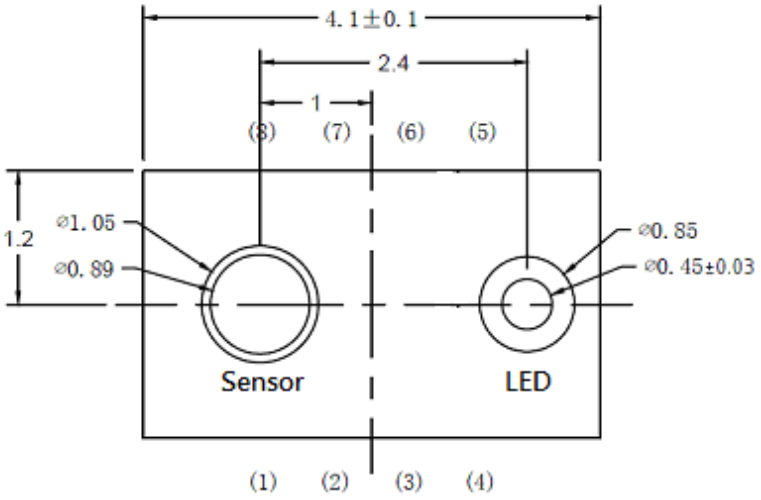
The PS Low Threshold registers are expressed as 10-bit data spread across two registers, PS Low Threshold Lower byte and PS Low Threshold higher byte.

PS low threshold = Reg_0x2B * 4 + Reg_0x2A

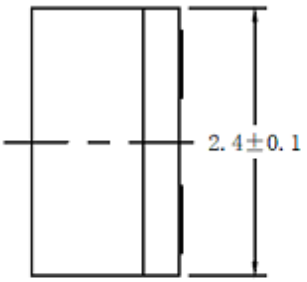
The PS High Threshold registers are expressed as 10-bit data spread across two registers, PS High Threshold Lower part and PS High Threshold higher part.

PS high threshold = Reg_0x2D * 4 + Reg_0x2C

Package Outline Dimensions

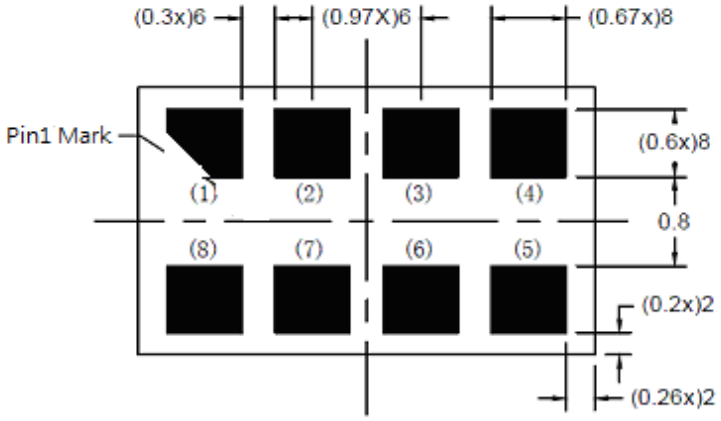


Top View



Right View

Side View



Bottom View

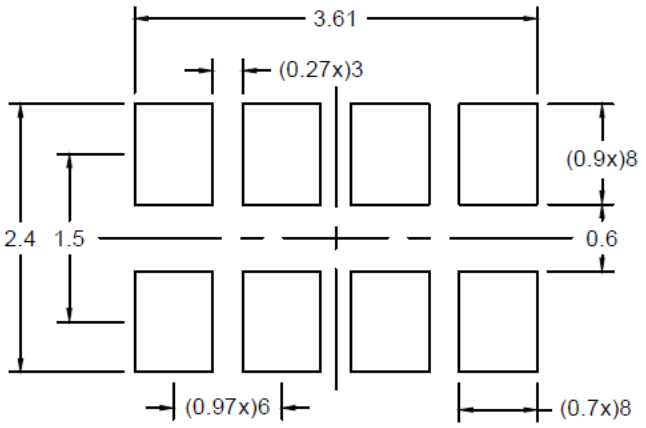
PINOUT:

1. VDD
2. SCL
3. GND
4. LEDA
5. LEDC
6. LDR
7. INT
8. SDA

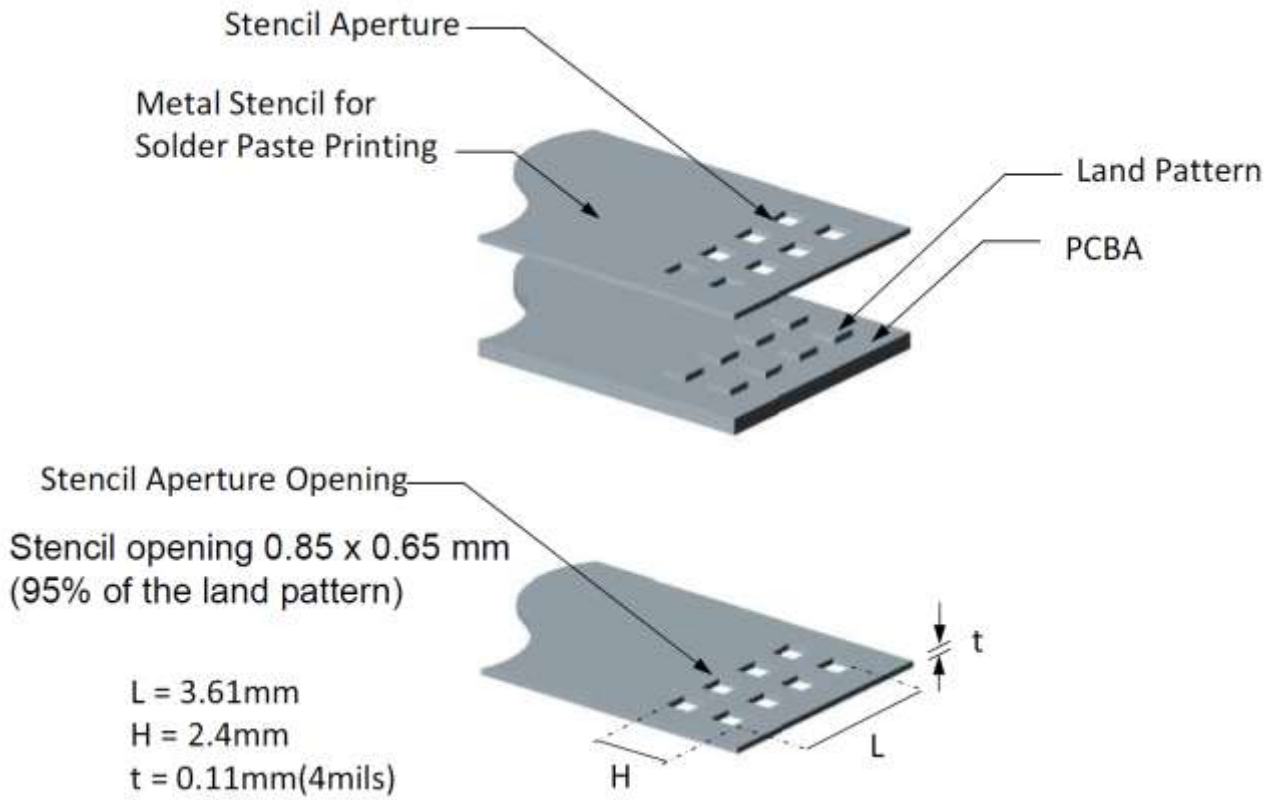
Notes:

All dimensions are in millimeters.

Recommended Land Pattern

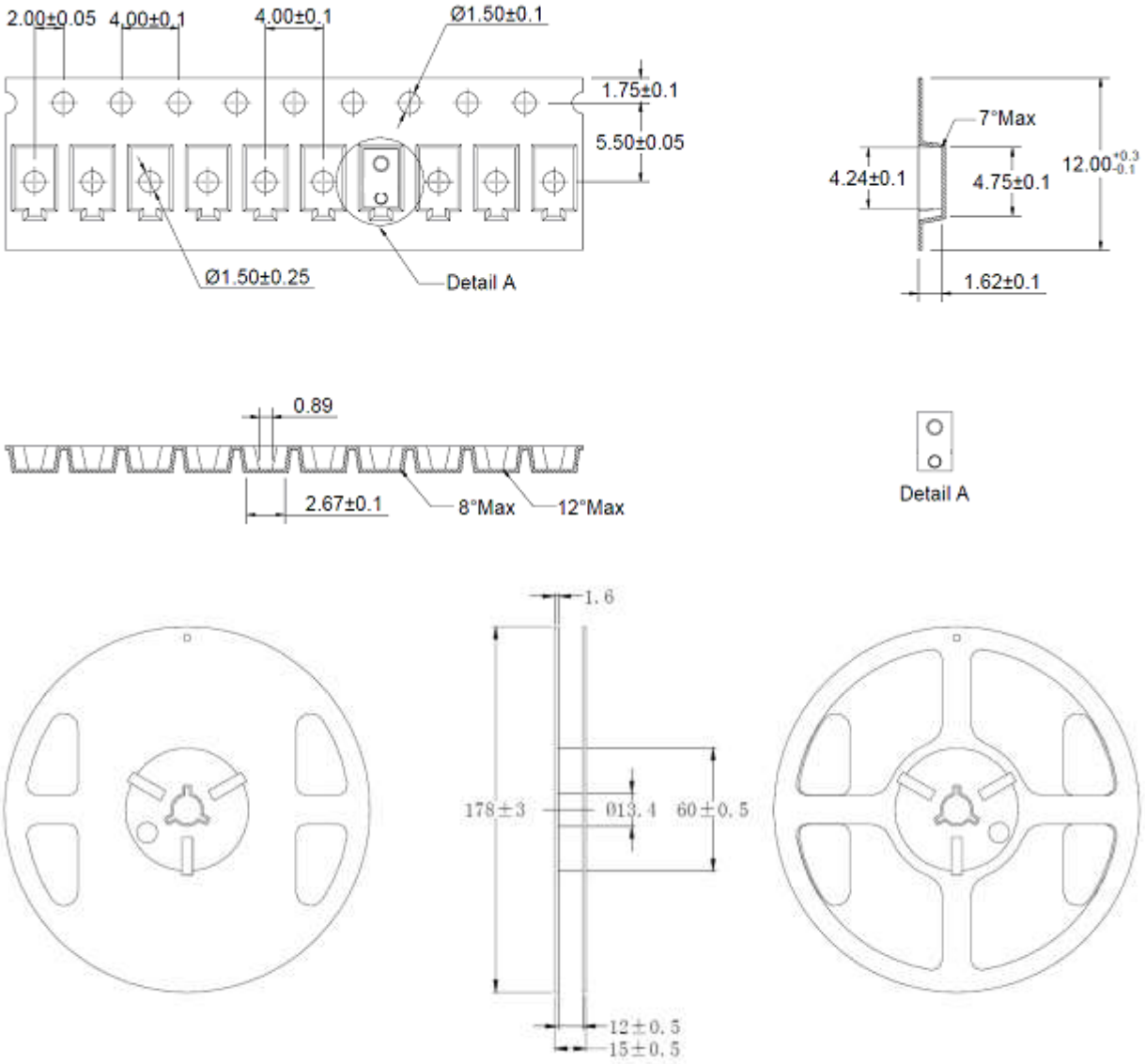


Stencil

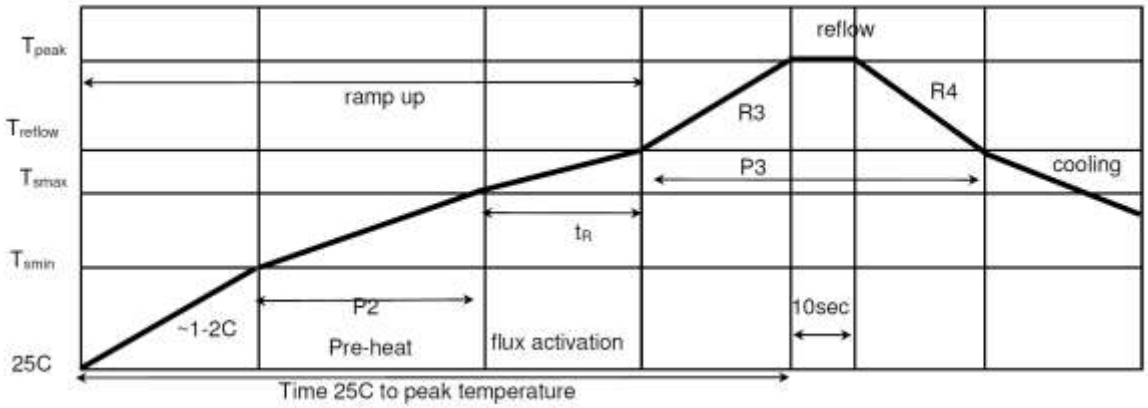


Note : The dimensions of stencil are designed base on the SMT process tolerance (less than +/-3° rotation and +/-0.05mm offset).

Package Dimension of Tape and Reel



Recommended Reflow Profile



	Peak temperature (Tpeak)	255-260C (max) ; 10sec
Pre-Heat	Temperature min (Tsmin) Temperature max (Tsmax) P2: (Ts min to Ts max)	150C 2C/sec 150C-217C 100s to 180s 90-110s
Time maintain above	Temperature (T_{reflow}) Time (P3) R3 slope (from 217C -> peak) R4 slope (from peak -> 217C)	217C 60-90sec 2C/sec [typ] -> 2.5C/sec (max) -1.5C/sec [typ]-> -4C/sec (max)
	Time to peak temperature	480s max
	Cooling down slope (peak to 217C)	2-4C/ sec

Note : The actual profile may need to be adjusted base on the actual layout. When parts are placed upside down, proper protection/support is recommended, max reflow should not exceed 2x max